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**10<sup>5</sup> PULSE HEIGHT ANALYZER FOR USE  
IN HIGH ENERGY  
COSMIC RAY EXPERIMENTS (HECRE)  
ON HIGH ALTITUDE BALLOON FLIGHTS**

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**GSFC**

**— GODDARD SPACE FLIGHT CENTER —  
GREENBELT, MARYLAND**

(NASA-TM-X-65836) A 100,000 PULSE HEIGHT  
ANALYZER FOR USE IN HIGH ENERGY COSMIC RAY  
EXPERIMENTS (HECRE) ON HIGH ALTITUDE  
BALLOON FLIGHTS C.A. Cancro, et al (NASA)  
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GODDARD SPACE FLIGHT CENTER  
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## INTRODUCTION

This report describes a wide dynamic range pulse height analyzer system developed for use on High Energy Cosmic Ray Experiment (HECRE) Balloon Flights. A wide dynamic range of 10<sup>5</sup> is obtained by extending the range of a basic 1024 channel analyzer through the use of multiple ranges and range selection. The system described here contains four 10<sup>5</sup> pulse height analyzers. Each 10<sup>5</sup> pulse height analyzer consists of a group of cordwood welded modules mounted and interconnected on a printed circuit card. Four of these card assemblies, the required clock drive circuitry (discrete components mounted and interconnected on a separate card) and three input-output connectors are interconnected and mounted on the system board, as shown in Figure 1.

## SYSTEM OPERATION

Reference (a) describes the general operation of a wide range pulse height analyzer which makes use of multiple ranges and range selection. The system developed for the HECRE Balloon Flights makes use of a basic 1024 channel analyzer and 4 separate ranges of X1, X1/5, X1/25 and X1/125. Figure 2 is a block diagram of this 10<sup>5</sup> pulse height analyzer. The four inputs (from the detector pre-amplifiers) feed identical delay and linear gate chains. The delay is provided to allow the instrumentation logic system (not described in this report) sufficient time to determine whether or not an event should be processed (pulse height analyzed) and the appropriate linear gate opened. The outputs of the four linear gates are connected in parallel and feed a single sweep. Essentially, the sweep converts the input pulse from the opened linear gate to an output pulse with a width proportional to the input pulse amplitude. This output pulse drives the P.H.A. (pulse height analyzer) output gate which then allows the pulses from a free running 500 kHz square wave oscillator to pass through to the output. Thus, the output pulse train will contain a total number of pulses proportional to the input pulse amplitude. As indicated in Figure 2, an enable pulse initiates the sweep and output pulse train. The enable pulse is of relatively short duration and is generated by the clock drive circuitry when the instrumentation logic indicates an event to be processed. This arrangement assures that the output pulse train always starts at the trailing edge of an oscillator pulse (eliminating jitter error) and that noise is very unlikely to generate spurious output pulse trains. It will be noted that the X1, X1/5 and X1/25 inputs from the detector

also drive top of range threshold detectors. The outputs from these threshold detectors feed the four range decision circuit. Also driving the four range decision circuit are a sequence of clock pulses. These are the reset, write and transfer clock pulses. These clock pulses are also generated by the clock drive circuitry when the instrumentation logic system indicates an event to be processed. The outputs of the four range decision circuit drive their associated linear gates. Thus, dependent on the range of the input signal, the appropriate top of range threshold detectors are actuated and through the four range decision circuit, the correct linear gate,  $X1$ ,  $X1/5$ ,  $X1/25$  or  $X1/125$  is opened. Bistables in the four range decision circuit generate the bits  $S1$  and  $S2$  which indicate which linear gate is opened and what multiplying factor is to be applied to the output pulse train count.

The linear range of input signals at all four inputs to the  $10^5$  pulse height analyzer is 2.5 millivolts to 2.0 volts with the input limited at 2.5 volts to prevent overdrive. The output pulse train yields one output pulse per 2.5 millivolts at the input. The thresholds of the  $X1$ ,  $X1/5$  and  $X1/25$  top of range threshold detectors are all set at 2.0 volts. Table 1 summarizes the characteristics of the  $10^5$  pulse height analyzer.

## $10^5$ PULSE HEIGHT ANALYZER INTERCONNECT

Figure 3 is an electrical interconnect diagram of one of the  $10^5$  pulse height analyzer assemblies. This shows the connections between the cordwood welded modules (shown as closed rectangles with terminals), delay lines, discrete components and input-output terminals. The  $X1$ ,  $X1/5$ ,  $X1/25$  and  $X1/125$  input signals from the detector come into terminals 14, 16, 20 and 18, respectively, and drive delay lines. The resistors in the input and output circuits of the delay lines (for example,  $R1$  and  $R2$  for delay line "A") are selected to match the impedance of the delay line. The inductors between pin 11 and common of the linear gates (for example,  $L1$  for linear gate "A") are selected to set the linear gate open time. In this system the inductance used with all four linear gates was 3300 microhenrys which yields a linear gate open time of approximately 6.0 microseconds. The capacitors connected across these inductors ( $C5$  through  $C8$ ) are selected to eliminate spurious linear gate outputs when the linear gates are opened. The  $X1$ ,  $X1/5$  and  $X1/25$  input signals also drive their respective top of range threshold detectors through attenuators (for example,  $R9-R10$  for the  $X1$  input signal). The three top of range threshold detectors are contained in a single module. The T.B.D. resistors in the attenuators are selected so that the input signal at the top of range threshold is 2.0 volts. Inductors  $L5$ ,  $L6$  and  $L7$  are selected to yield output pulses of approximately 6.0 microseconds at or above the top of range threshold. The value of inductance for  $L5$ ,  $L6$  and  $L7$  is 3300 microhenrys.

Table 1  
10<sup>5</sup> Pulse Height Analyzer Characteristics

	Range I	Range II	Range III	Range IV
Input to Detector (channel)	1-800	800-4000	4000-20,000	20,000-100,000
Detector X1 Input (mv.)	2.5-2000	Limited 2.5v	Limited 2.5v	Limited 2.5v
Detector X1/5 Input (mv.)	0.5-400	400-2000	Limited 2.5v	Limited 2.5v
Detector X1/25 Input (mv.)	0.1-80	80-400	400-2000	Limited 2.5v
Detector X1/125 Input (mv.)	0.02-16	16-80	80-400	400-2000
S1 Bit	0	1	0	1
S2 Bit	0	0	1	1
Open Linear Gate	X1	X1/5	X1/25	X1/125
Multiply Output Pulse Train By	1	5	25	125

#### PRINTED CIRCUIT BOARD

Figure 4 is the printed circuit card artwork for the 10<sup>5</sup> pulse height analyzer. This card has printed circuitry on both sides.

#### LINEAR GATE

Figure 5 is an electrical schematic diagram of the linear gate module. A detailed description of the linear gate is given in reference (b). The shaper section is deleted in this application since the detector pre-amplifiers shape the input

signal. The signal at the output of the linear gate when open, is twice that at the input to the  $10^5$  pulse height analyzer. Thus, the 2.5 millivolts to 2.0 volts range is converted to 5.0 millivolts to 4.0 volts at the output of the linear gate. The gain of transistor amplifier stages Q1-Q2 is adjusted by selection of R-8 to obtain this output.

## SWEEP

Figure 6 is an electrical schematic diagram of the sweep module. A detailed description of the sweep circuit is given in reference (b). In this application, a tunnel diode (CR-12, Figure 6) has been included at output 2 to interface with the circuitry in the P.H.A. output gate. As indicated previously, the input linear range of signals to the sweep is 5.0 millivolts to 4.0 volts. The sweep output pulse width, effectively driving the P.H.A. output gate, is 2.0 microseconds per 5.0 millivolts of the input.

## P.H.A. OUTPUT GATE

Figure 7 is an electrical schematic diagram of the P.H.A. output gate module. The function of this module is to:

- a. initiate the 500 kHz output pulse train when there is an enable pulse coincident with a signal from the sweep,
- b. generate an output to start the sweep capacitor discharge at the instant the 500 kHz output pulse train is initiated and
- c. terminate the 500 kHz output pulse train at the instant the signal from the sweep returns to zero.

Transistor stages Q1 and Q2 convert the sweep output voltage swing of 0.0 volts to +0.5 volts into terminal 8 to the voltage swing of 0.0 volts to -0.24 across R5, as required by the following circuitry. With 0.0 volts at terminal 8, Q2 conducts and Q1 is cut off since Q2 base is at common while half the voltage at the collector of Q2 is fed back to the base of Q1. With Q1 not conducting, the voltage across R5 is zero. With +0.5 volts at terminal 8, Q1 is conducting and Q2 is cut off since the base of Q1 is at a more positive voltage than the base of Q2. The approximately 1.0 milliamperes of current flowing in the collector circuit of Q1 yields -0.24 across R5. The voltage across R5 is fed to the base of Q3. This is one input of the two input NAND gate consisting of transistor stages of Q3, Q4 and Q5. The enable input pulse feeds the base of Q4, which is the

second input to the NAND gate. The common emitters at Q3, Q4 and Q5 are driven by the constant current of 1.0 milliampere through R8. The common collectors of Q3 and Q4 are connected to R7 and the voltage developed across R7 is fed to the base of Q5. When either base of Q3 or Q4 is at zero volts, its collector to emitter circuit conducts and a voltage of -0.24 volts is developed across R7. This voltage fed to the base of Q5, cuts off Q5. When the voltage on both bases of Q3 and Q4 is -0.24 volts, these transistors are cut off with the voltage across R7 at zero volts. This zero voltage fed to the base of Q5, causes Q5 to conduct. Thus, when both a signal from the sweep (-0.24 volts on Q3 base) and the enable input (-0.24 volts on Q4 base) are present, the voltage across R7 is zero. The zero voltage across R7, fed to the base of Q6, sets the flip-flop consisting of transistor stages Q6, Q7, Q8 and Q9. This flip-flop consists of two cross coupled NAND gates with the set signal coming into the base of Q6 and the reset signal coming into the base of Q9. The outputs are taken across R9 and R10. The reset signal to the base of Q9 comes from the sweep output inverted signal across R5. Thus, the flip-flop is held in reset with no output from the sweep and is set when a signal is received from both the sweep and enable, and then reset when the sweep output returns to zero. The output from the flip-flop across R9 is fed to the base of Q15. This is one input of a two input NAND gate consisting of transistor stages Q13, Q14 and Q15. The second input comes from the free running 500 kHz square wave oscillator. The output of this NAND gate, across R25, is the square wave pulse train existing while the flip-flop is in the set stage. The output is fed through the level shifter, consisting of transistor stages Q10 and Q11, and drives output transistor Q12. The signal at the base of Q10 swings between zero and -0.24 volts. At zero volts, Q10 conducts, yielding a voltage of -0.24 volts across R13. This voltage fed to the base of Q11, cuts off Q11. Q12 is turned on by the current flowing into its base to emitter circuit through R14. For -0.24 volts on the base of Q10, Q10 is cut off and Q11 conducts. The resultant -0.5 volts on the collector of Q11 and base of Q12, cuts off Q12. Thus, the pulse train output is obtained at terminal 10 with Q12 turning on and off at the pulse train frequency. This arrangement allows a wide range of resistors and voltages to be connected to pin 10 so that a wide variety of TTL, DTL, MOS or CMOS counters may be driven. The second output from the Q6, Q7, Q8 and Q9 flip-flop, across R10, drives the level shifter consisting of transistor stages Q16-Q17. This is similar to the level shifter described previously. The output, from across R22, drives the Q18-Q19 amplifier stage. The output from this stage through terminal 11 goes to the sweep to control the sweep capacitor discharge. With the flip-flop reset (no sweep output), a voltage of approximately -2.0 volts is obtained at terminal 11, holding off the sweep capacitor discharge. With the flip-flop set (sweep and enable signals), a voltage of approximately +2.0 volts is obtained at terminal 11, allowing the sweep capacitor to discharge.

## THRESHOLD DETECTOR AND PULSER

Figure 8 is an electrical schematic diagram of the threshold detector and pulser module. This contains three separate threshold detector and pulse circuits. This circuitry is described in detail in reference (c). The threshold level of these detectors is approximately 220 millivolts.

## FOUR RANGE DECISION CIRCUIT

Figure 9 is an electrical schematic diagram of the four range decision circuit module. As indicated previously, the function of this circuitry is to open the appropriate linear gate and indicate the multiplying factor to be applied when an event is processed. The logic required in performing this function is given in reference (a) and a logic diagram for this module is shown in Figure 3. Figure 9 shows that the logic required is obtained in this module by use of the NAND gate, bistables and level shifter circuits described previously for the P.H.A. output gate module. It will be noted that the basic gate circuit, in addition to yielding the NAND function, also yields the AND function (for example, across R8, R16, R25 and R32).

## MODULE ARTWORK DRAWINGS

Table 2 lists the GSFC artwork drawing numbers from which the  $10^5$  pulse height analyzer cordwood welded modules were fabricated.

Table 2  
Module Artwork Drawing Numbers

Unit	GSFC Drawing
Linear Gate	02-400B
Sweep	02-401B
P.H.A. Output Gate	02-430A
Threshold Detector and Pulser	02-422B
Four Range Decision Circuit	02-427B



## CLOCK DRIVE CIRCUITRY

As indicated in Figure 3, the  $10^5$  pulse height analyzer requires inputs of:

- a. 500 kHz oscillator square wave pulses,
- b. the enable pulse and
- c. the reset, write and transfer clock pulses.

These inputs are provided by the clock drive circuitry which is made up of discrete components and is assembled on a miniature terminal card. This card is mounted at the rear of the system board as shown in Figure 1.

Figure 10 is an electrical schematic diagram of the 500 kHz square wave oscillator and spiker circuitry mounted on the clock drive card. Transistor stage Q1 is a standard sine wave crystal oscillator. The sine wave output is fed to the base of Q2. Q2 and Q3 share a common emitter resistor R7. Q3 base is connected to common. As the sine wave input to the base of Q2 crosses zero voltage in each direction Q3 conducts and is cut off alternately. This causes tunnel diode CR1 to switch between its high and low voltage states, yielding a square wave output. Resistor R8 is selected to set the d.c. bias on the base of Q2 to obtain a square wave at the output. This output is fed to the Q4 - Q5 pulse generator stage. This pulse generator, described in detail in reference (c), generates a spike at the junction of CR2 - CR-3 coincident with the trailing edge of the square wave.

Figure 11 is an electrical schematic diagram of the clock and buffer circuits mounted on the clock drive card. The function of these circuits is to:

- a. generate the reset, write and transfer clock pulses in sequence upon receiving an input signal from the instrumentation logic system (indicating an event to be processed),
- b. generate the output gate enable pulse and
- c. buffer the 500 kHz square wave, enable pulse, reset, write and transfer clock pulse outputs to provide voltage and impedance match to the inputs in the four  $10^5$  pulse height analyzers.

When the instrumentation logic system determines that an event is to be processed (pulse height analyzed), a positive pulse is applied into terminal E5. The Q1 - Q2 buffer stage converts this positive input pulse to a negative pulse across R1

as required for operation of the following circuitry. The Q1-Q2 stage is similar to that for the P.H.A. output gate. The negative pulse across R1 drives both a spiker and a 5 microsecond delay pulse generator. The spiker, consisting of transistor stages Q3 and Q4, generates a normalized spike for each input pulse and drives the three series connected pulse generators Q5-Q6, Q7-Q8 and Q9-Q10. The spiker and pulse generator circuitry is described in detail in reference (c). These generate the reset, write and transfer clock pulses in sequence. The width of each of these pulses is adjusted by selection of L2, L3 and L4 to 200 nanoseconds. The reset, write and transfer pulse outputs from the generators go through their respective buffer circuits (Q11-Q12, Q13-Q14 and Q15-Q16) and on through terminals E7, E6 and E9 to the four  $10^5$  pulse height analyzers. The buffer circuits consist of a one input AND gate of the type described previously with low output impedances of 51 ohms so as to readily drive the four  $10^5$  pulse height analyzers.

The 5 microsecond delay pulse generator consists of transistor stages Q17 and Q18. This generates a 3 microsecond pulse delayed 5 microseconds after the event process input signal. This pulse generator is described in reference (c). The delayed 3 microsecond pulse is fed into one input of the two input AND gate consisting of transistor stages Q19, Q20 and Q21. The spiker from the 500 kHz square wave oscillator, described previously, is fed into the second input of the AND gate. The output of this AND gate is generated across R47 and is the enable pulse. Thus, the enable pulse is generated at the trailing edge of the first 500 kHz square wave oscillator pulse occurring 5 microseconds after the event process pulse is obtained from the instrumentation system logic.

The arrangement described above assures that:

- a. the sweep capacitor in the sweep circuit is fully charged to the peak of the input signal voltage before sweep discharge begins (because of the 5 microseconds delay),
- b. the output pulse train always starts at the trailing edge of an oscillator pulse, thus eliminating jitter error in the output pulse train count, and
- c. no spurious output pulse trains will be generated since the output pulse train may be initiated only during the 3 microsecond period following the event process input pulse with a sweep output signal present.

The enable pulse is fed through the buffer stage Q22-Q23 and out through terminal E8 to the four  $10^5$  pulse height analyzers. Buffer stage Q24-Q25

buffers the 500 kHz square wave oscillator through terminal E10 to the four  $10^5$  pulse height analyzers.

#### SYSTEM BOARD INTERCONNECTIONS

Figure 12 is an electrical interconnect diagram of the four  $10^5$  pulse height analyzer cards, the clock drive card and the input-output connectors.

#### POWER DRAIN

Table 3 lists the current and power drain of the assembled system.

(Table 3)

$10^5$  Pulse Height Analyzer System Current and Power Drain

Voltage	Current Drain (milliamperes)	Power Drain (milliwatts)
+12.0	0.6	7.2
+6.25	9.8	61.3
+2.25	39.0	87.8
-2.25	135.0	304.0
-6.25	15.8	98.8
-12.0	8.8	105.6
Total		664.7

#### TEMPERATURE CHARACTERISTICS

The assembled system board operated satisfactorily in the temperature range  $-10^{\circ}\text{C}$  to  $+40^{\circ}\text{C}$ .

## REFERENCES

- a. Ciro A. Cancro, "Wide Range Pulse Height Analyzer With Data Compression Readout for Satellite Application," GSFC Report X-711-68-402, Nuclear Instruments and Methods, 73 (1969), pp. 61-66.
- b. Ciro A. Cancro and Norman M. Garrahan, "Pulse Height Analyzer and Associated Threshold Detection and Logic Circuitry for General Satellite Application," GSFC Report X-711-68-274, Nuclear Instruments and Methods, Vol. 70:3 (1969) pp. 245-252.
- c. Ciro A. Cancro, "Fast Low-Power-Drain Logic System for Use in Nuclear Experiments on Scientific Satellites," GSFC Report X-711-70-201, IEEE Transactions on Nuclear Science, October 1970, pp. 3-7.

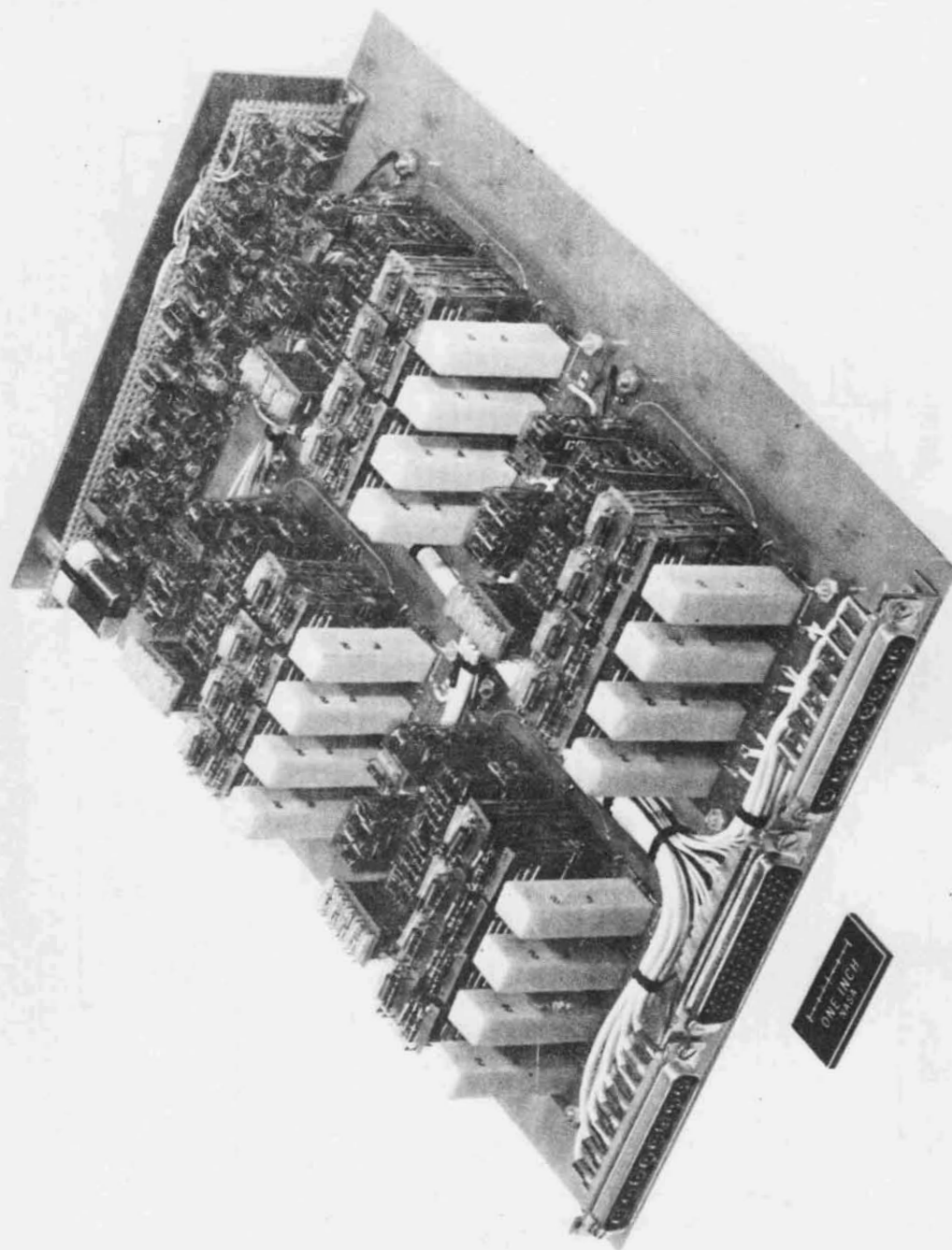


Figure 1. 10<sup>5</sup> Pulse Height Analyzer System Board

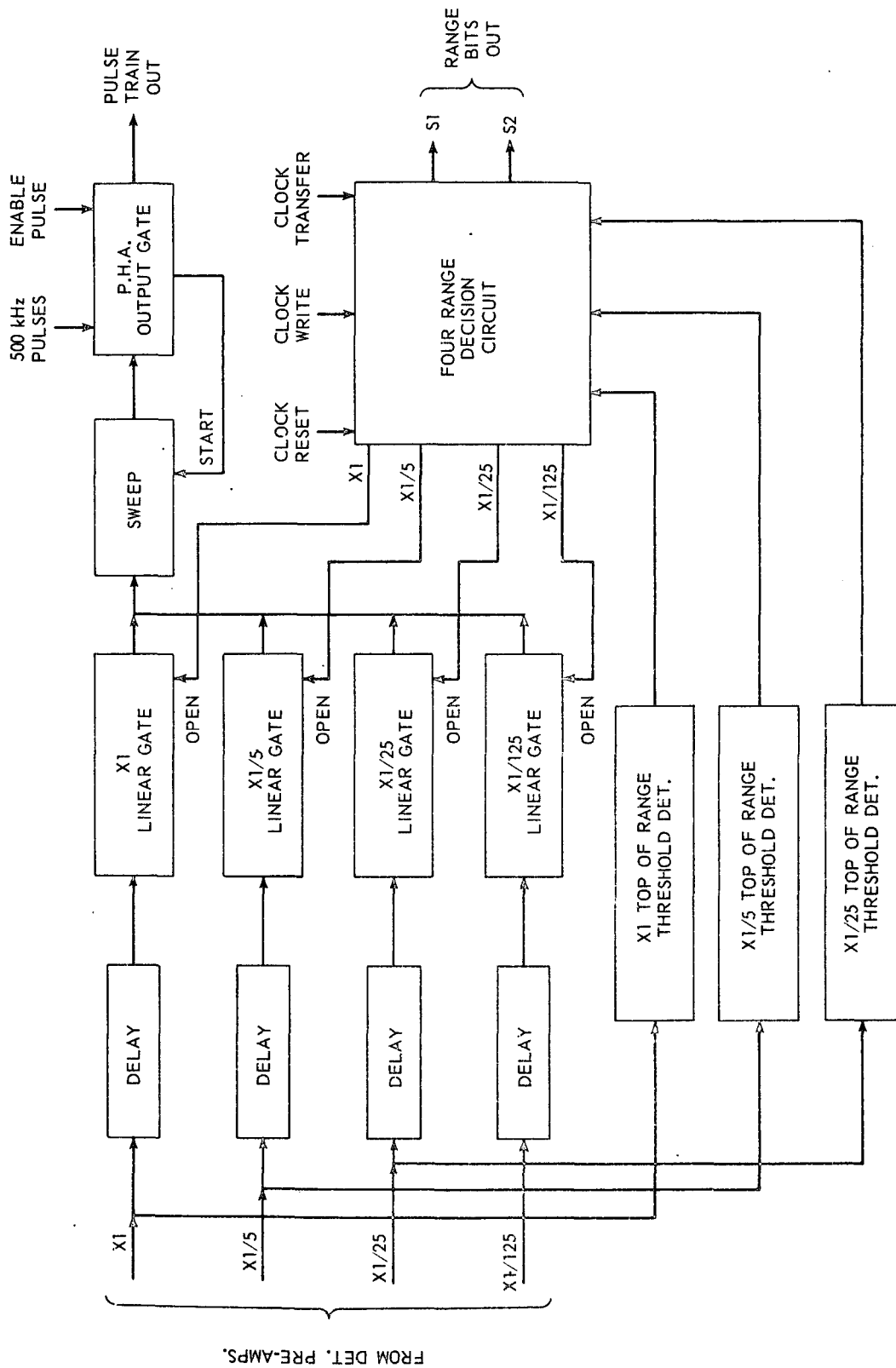


Figure 2.  $10^5$  Pulse Height Analyzer, Block Diagram

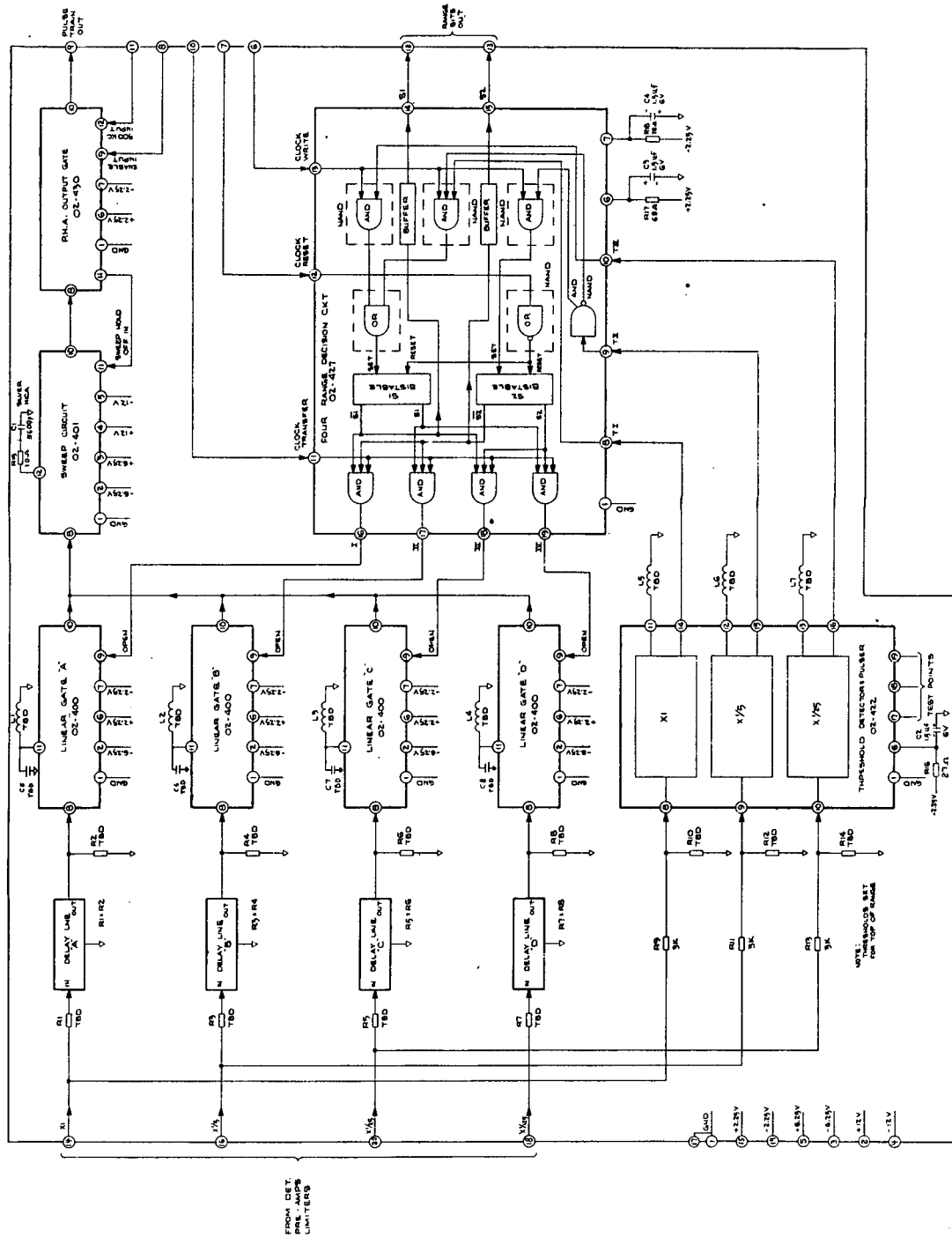


Figure 3.  $10^5$  Pulse Height Analyzer, Electrical Interconnect Diagram



Figure 4.  $10^5$  Pulse Height Analyzer, Printed Circuit Card Artwork

DESIGNATION	DESCRIPTION
A1, A2, A3, A4	ATOMIC TALK, 1500 WATT
Q1, Q2, Q3, Q4	6Z-450 LINEAR GATE
Q5, Q6, Q7, Q8	6Z-450 LINEAR GATE
Q9, Q10, Q11, Q12	6Z-450 THRESHOLD DET. PULSER,
Q13, Q14, Q15, Q16	6Z-450 THRESHOLD DET. PULSER,
Q17, Q18, Q19, Q20	6Z-450 P.A. OUTPUT GATE.
Q21, Q22, Q23, Q24	6Z-450 P.A. OUTPUT GATE.
Q25, Q26, Q27, Q28	6Z-450 P.A. OUTPUT GATE.
Q29, Q30, Q31, Q32	6Z-450 P.A. OUTPUT GATE.
Q33, Q34, Q35, Q36	6Z-450 P.A. OUTPUT GATE.
Q37, Q38, Q39, Q40	6Z-450 P.A. OUTPUT GATE.
Q41, Q42, Q43, Q44	6Z-450 P.A. OUTPUT GATE.
Q45, Q46, Q47, Q48	6Z-450 P.A. OUTPUT GATE.
Q49, Q50, Q51, Q52	6Z-450 P.A. OUTPUT GATE.
Q53, Q54, Q55, Q56	6Z-450 P.A. OUTPUT GATE.
Q57, Q58, Q59, Q60	6Z-450 P.A. OUTPUT GATE.
Q61, Q62, Q63, Q64	6Z-450 P.A. OUTPUT GATE.
Q65, Q66, Q67, Q68	6Z-450 P.A. OUTPUT GATE.
Q69, Q70, Q71, Q72	6Z-450 P.A. OUTPUT GATE.
Q73, Q74, Q75, Q76	6Z-450 P.A. OUTPUT GATE.
Q77, Q78, Q79, Q80	6Z-450 P.A. OUTPUT GATE.
Q81, Q82, Q83, Q84	6Z-450 P.A. OUTPUT GATE.
Q85, Q86, Q87, Q88	6Z-450 P.A. OUTPUT GATE.
Q89, Q90, Q91, Q92	6Z-450 P.A. OUTPUT GATE.
Q93, Q94, Q95, Q96	6Z-450 P.A. OUTPUT GATE.
Q97, Q98, Q99, Q100	6Z-450 P.A. OUTPUT GATE.
Q101, Q102, Q103, Q104	6Z-450 P.A. OUTPUT GATE.
Q105, Q106, Q107, Q108	6Z-450 P.A. OUTPUT GATE.
Q109, Q110, Q111, Q112	6Z-450 P.A. OUTPUT GATE.
Q113, Q114, Q115, Q116	6Z-450 P.A. OUTPUT GATE.
Q117, Q118, Q119, Q120	6Z-450 P.A. OUTPUT GATE.
Q121, Q122, Q123, Q124	6Z-450 P.A. OUTPUT GATE.
Q125, Q126, Q127, Q128	6Z-450 P.A. OUTPUT GATE.
Q129, Q130, Q131, Q132	6Z-450 P.A. OUTPUT GATE.
Q133, Q134, Q135, Q136	6Z-450 P.A. OUTPUT GATE.
Q137, Q138, Q139, Q140	6Z-450 P.A. OUTPUT GATE.
Q141, Q142, Q143, Q144	6Z-450 P.A. OUTPUT GATE.
Q145, Q146, Q147, Q148	6Z-450 P.A. OUTPUT GATE.
Q149, Q150, Q151, Q152	6Z-450 P.A. OUTPUT GATE.
Q153, Q154, Q155, Q156	6Z-450 P.A. OUTPUT GATE.
Q157, Q158, Q159, Q160	6Z-450 P.A. OUTPUT GATE.
Q161, Q162, Q163, Q164	6Z-450 P.A. OUTPUT GATE.
Q165, Q166, Q167, Q168	6Z-450 P.A. OUTPUT GATE.
Q169, Q170, Q171, Q172	6Z-450 P.A. OUTPUT GATE.
Q173, Q174, Q175, Q176	6Z-450 P.A. OUTPUT GATE.
Q177, Q178, Q179, Q180	6Z-450 P.A. OUTPUT GATE.
Q181, Q182, Q183, Q184	6Z-450 P.A. OUTPUT GATE.
Q185, Q186, Q187, Q188	6Z-450 P.A. OUTPUT GATE.
Q189, Q190, Q191, Q192	6Z-450 P.A. OUTPUT GATE.
Q193, Q194, Q195, Q196	6Z-450 P.A. OUTPUT GATE.
Q197, Q198, Q199, Q200	6Z-450 P.A. OUTPUT GATE.
Q201, Q202, Q203, Q204	6Z-450 P.A. OUTPUT GATE.
Q205, Q206, Q207, Q208	6Z-450 P.A. OUTPUT GATE.
Q209, Q210, Q211, Q212	6Z-450 P.A. OUTPUT GATE.
Q213, Q214, Q215, Q216	6Z-450 P.A. OUTPUT GATE.
Q217, Q218, Q219, Q220	6Z-450 P.A. OUTPUT GATE.
Q221, Q222, Q223, Q224	6Z-450 P.A. OUTPUT GATE.
Q225, Q226, Q227, Q228	6Z-450 P.A. OUTPUT GATE.
Q229, Q230, Q231, Q232	6Z-450 P.A. OUTPUT GATE.
Q233, Q234, Q235, Q236	6Z-450 P.A. OUTPUT GATE.
Q237, Q238, Q239, Q240	6Z-450 P.A. OUTPUT GATE.
Q241, Q242, Q243, Q244	6Z-450 P.A. OUTPUT GATE.
Q245, Q246, Q247, Q248	6Z-450 P.A. OUTPUT GATE.
Q249, Q250, Q251, Q252	6Z-450 P.A. OUTPUT GATE.
Q253, Q254, Q255, Q256	6Z-450 P.A. OUTPUT GATE.
Q257, Q258, Q259, Q260	6Z-450 P.A. OUTPUT GATE.
Q261, Q262, Q263, Q264	6Z-450 P.A. OUTPUT GATE.
Q265, Q266, Q267, Q268	6Z-450 P.A. OUTPUT GATE.
Q269, Q270, Q271, Q272	6Z-450 P.A. OUTPUT GATE.
Q273, Q274, Q275, Q276	6Z-450 P.A. OUTPUT GATE.
Q277, Q278, Q279, Q280	6Z-450 P.A. OUTPUT GATE.
Q281, Q282, Q283, Q284	6Z-450 P.A. OUTPUT GATE.
Q285, Q286, Q287, Q288	6Z-450 P.A. OUTPUT GATE.
Q289, Q290, Q291, Q292	6Z-450 P.A. OUTPUT GATE.
Q293, Q294, Q295, Q296	6Z-450 P.A. OUTPUT GATE.
Q297, Q298, Q299, Q300	6Z-450 P.A. OUTPUT GATE.
Q301, Q302, Q303, Q304	6Z-450 P.A. OUTPUT GATE.
Q305, Q306, Q307, Q308	6Z-450 P.A. OUTPUT GATE.
Q309, Q310, Q311, Q312	6Z-450 P.A. OUTPUT GATE.
Q313, Q314, Q315, Q316	6Z-450 P.A. OUTPUT GATE.
Q317, Q318, Q319, Q320	6Z-450 P.A. OUTPUT GATE.
Q321, Q322, Q323, Q324	6Z-450 P.A. OUTPUT GATE.
Q325, Q326, Q327, Q328	6Z-450 P.A. OUTPUT GATE.
Q329, Q330, Q331, Q332	6Z-450 P.A. OUTPUT GATE.
Q333, Q334, Q335, Q336	6Z-450 P.A. OUTPUT GATE.
Q337, Q338, Q339, Q340	6Z-450 P.A. OUTPUT GATE.
Q341, Q342, Q343, Q344	6Z-450 P.A. OUTPUT GATE.
Q345, Q346, Q347, Q348	6Z-450 P.A. OUTPUT GATE.
Q349, Q350, Q351, Q352	6Z-450 P.A. OUTPUT GATE.
Q353, Q354, Q355, Q356	6Z-450 P.A. OUTPUT GATE.
Q357, Q358, Q359, Q360	6Z-450 P.A. OUTPUT GATE.
Q361, Q362, Q363, Q364	6Z-450 P.A. OUTPUT GATE.
Q365, Q366, Q367, Q368	6Z-450 P.A. OUTPUT GATE.
Q369, Q370, Q371, Q372	6Z-450 P.A. OUTPUT GATE.
Q373, Q374, Q375, Q376	6Z-450 P.A. OUTPUT GATE.
Q377, Q378, Q379, Q380	6Z-450 P.A. OUTPUT GATE.
Q381, Q382, Q383, Q384	6Z-450 P.A. OUTPUT GATE.
Q385, Q386, Q387, Q388	6Z-450 P.A. OUTPUT GATE.
Q389, Q390, Q391, Q392	6Z-450 P.A. OUTPUT GATE.
Q393, Q394, Q395, Q396	6Z-450 P.A. OUTPUT GATE.
Q397, Q398, Q399, Q400	6Z-450 P.A. OUTPUT GATE.
Q401, Q402, Q403, Q404	6Z-450 P.A. OUTPUT GATE.
Q405, Q406, Q407, Q408	6Z-450 P.A. OUTPUT GATE.
Q409, Q410, Q411, Q412	6Z-450 P.A. OUTPUT GATE.
Q413, Q414, Q415, Q416	6Z-450 P.A. OUTPUT GATE.
Q417, Q418, Q419, Q420	6Z-450 P.A. OUTPUT GATE.
Q421, Q422, Q423, Q424	6Z-450 P.A. OUTPUT GATE.
Q425, Q426, Q427, Q428	6Z-450 P.A. OUTPUT GATE.
Q429, Q430, Q431, Q432	6Z-450 P.A. OUTPUT GATE.
Q433, Q434, Q435, Q436	6Z-450 P.A. OUTPUT GATE.
Q437, Q438, Q439, Q440	6Z-450 P.A. OUTPUT GATE.
Q441, Q442, Q443, Q444	6Z-450 P.A. OUTPUT GATE.
Q445, Q446, Q447, Q448	6Z-450 P.A. OUTPUT GATE.
Q449, Q450, Q451, Q452	6Z-450 P.A. OUTPUT GATE.
Q453, Q454, Q455, Q456	6Z-450 P.A. OUTPUT GATE.
Q457, Q458, Q459, Q460	6Z-450 P.A. OUTPUT GATE.
Q461, Q462, Q463, Q464	6Z-450 P.A. OUTPUT GATE.
Q465, Q466, Q467, Q468	6Z-450 P.A. OUTPUT GATE.
Q469, Q470, Q471, Q472	6Z-450 P.A. OUTPUT GATE.
Q473, Q474, Q475, Q476	6Z-450 P.A. OUTPUT GATE.
Q477, Q478, Q479, Q480	6Z-450 P.A. OUTPUT GATE.
Q481, Q482, Q483, Q484	6Z-450 P.A. OUTPUT GATE.
Q485, Q486, Q487, Q488	6Z-450 P.A. OUTPUT GATE.
Q489, Q490, Q491, Q492	6Z-450 P.A. OUTPUT GATE.
Q493, Q494, Q495, Q496	6Z-450 P.A. OUTPUT GATE.
Q497, Q498, Q499, Q500	6Z-450 P.A. OUTPUT GATE.
Q501, Q502, Q503, Q504	6Z-450 P.A. OUTPUT GATE.
Q505, Q506, Q507, Q508	6Z-450 P.A. OUTPUT GATE.
Q509, Q510, Q511, Q512	6Z-450 P.A. OUTPUT GATE.
Q513, Q514, Q515, Q516	6Z-450 P.A. OUTPUT GATE.
Q517, Q518, Q519, Q520	6Z-450 P.A. OUTPUT GATE.
Q521, Q522, Q523, Q524	6Z-450 P.A. OUTPUT GATE.
Q525, Q526, Q527, Q528	6Z-450 P.A. OUTPUT GATE.
Q529, Q530, Q531, Q532	6Z-450 P.A. OUTPUT GATE.
Q533, Q534, Q535, Q536	6Z-450 P.A. OUTPUT GATE.
Q537, Q538, Q539, Q540	6Z-450 P.A. OUTPUT GATE.
Q541, Q542, Q543, Q544	6Z-450 P.A. OUTPUT GATE.
Q545, Q546, Q547, Q548	6Z-450 P.A. OUTPUT GATE.
Q549, Q550, Q551, Q552	6Z-450 P.A. OUTPUT GATE.
Q553, Q554, Q555, Q556	6Z-450 P.A. OUTPUT GATE.
Q557, Q558, Q559, Q560	6Z-450 P.A. OUTPUT GATE.
Q561, Q562, Q563, Q564	6Z-450 P.A. OUTPUT GATE.
Q565, Q566, Q567, Q568	6Z-450 P.A. OUTPUT GATE.
Q569, Q570, Q571, Q572	6Z-450 P.A. OUTPUT GATE.
Q573, Q574, Q575, Q576	6Z-450 P.A. OUTPUT GATE.
Q577, Q578, Q579, Q580	6Z-450 P.A. OUTPUT GATE.
Q581, Q582, Q583, Q584	6Z-450 P.A. OUTPUT GATE.
Q585, Q586, Q587, Q588	6Z-450 P.A. OUTPUT GATE.
Q589, Q590, Q591, Q592	6Z-450 P.A. OUTPUT GATE.
Q593, Q594, Q595, Q596	6Z-450 P.A. OUTPUT GATE.
Q597, Q598, Q599, Q600	6Z-450 P.A. OUTPUT GATE.
Q601, Q602, Q603, Q604	6Z-450 P.A. OUTPUT GATE.
Q605, Q606, Q607, Q608	6Z-450 P.A. OUTPUT GATE.
Q609, Q610, Q611, Q612	6Z-450 P.A. OUTPUT GATE.
Q613, Q614, Q615, Q616	6Z-450 P.A. OUTPUT GATE.
Q617, Q618, Q619, Q620	6Z-450 P.A. OUTPUT GATE.
Q621, Q622, Q623, Q624	6Z-450 P.A. OUTPUT GATE.
Q625, Q626, Q627, Q628	6Z-450 P.A. OUTPUT GATE.
Q629, Q630, Q631, Q632	6Z-450 P.A. OUTPUT GATE.
Q633, Q634, Q635, Q636	6Z-450 P.A. OUTPUT GATE.
Q637, Q638, Q639, Q640	6Z-450 P.A. OUTPUT GATE.
Q641, Q642, Q643, Q644	6Z-450 P.A. OUTPUT GATE.
Q645, Q646, Q647, Q648	6Z-450 P.A. OUTPUT GATE.
Q649, Q650, Q651, Q652	6Z-450 P.A. OUTPUT GATE.
Q653, Q654, Q655, Q656	6Z-450 P.A. OUTPUT GATE.
Q657, Q658, Q659, Q660	6Z-450 P.A. OUTPUT GATE.
Q661, Q662, Q663, Q664	6Z-450 P.A. OUTPUT GATE.
Q665, Q666, Q667, Q668	6Z-450 P.A. OUTPUT GATE.
Q669, Q670, Q671, Q672	6Z-450 P.A. OUTPUT GATE.
Q673, Q674, Q675, Q676	6Z-450 P.A. OUTPUT GATE.
Q677, Q678, Q679, Q680	6Z-450 P.A. OUTPUT GATE.
Q681, Q682, Q683, Q684	6Z-450 P.A. OUTPUT GATE.
Q685, Q686, Q687, Q688	6Z-450 P.A. OUTPUT GATE.
Q689, Q690, Q691, Q692	6Z-450 P.A. OUTPUT GATE.
Q693, Q694, Q695, Q696	6Z-450 P.A. OUTPUT GATE.
Q697, Q698, Q699, Q700	6Z-450 P.A. OUTPUT GATE.
Q701, Q702, Q703, Q704	6Z-450 P.A. OUTPUT GATE.
Q705, Q706, Q707, Q708	6Z-450 P.A. OUTPUT GATE.
Q709, Q710, Q711, Q712	6Z-450 P.A. OUTPUT GATE.
Q713, Q714, Q715, Q716	6Z-450 P.A. OUTPUT GATE.
Q717, Q718, Q719, Q720	6Z-450 P.A. OUTPUT GATE.
Q721, Q722, Q723, Q724	6Z-450 P.A. OUTPUT GATE.
Q725, Q726, Q727, Q728	6Z-450 P.A. OUTPUT GATE.
Q729, Q730, Q731, Q732	6Z-450 P.A. OUTPUT GATE.
Q733, Q734, Q735, Q736	6Z-450 P.A. OUTPUT GATE.
Q737, Q738, Q739, Q740	6Z-450 P.A. OUTPUT GATE.
Q741, Q742, Q743, Q744	6Z-450 P.A. OUTPUT GATE.
Q745, Q746, Q747, Q748	6Z-450 P.A. OUTPUT GATE.
Q749, Q750, Q751, Q752	6Z-450 P.A. OUTPUT GATE.
Q753, Q754, Q755, Q756	6Z-450 P.A. OUTPUT GATE.
Q757, Q758, Q759, Q760	6Z-450 P.A. OUTPUT GATE.
Q761, Q762, Q763, Q764	6Z-450 P.A. OUTPUT GATE.
Q765, Q766, Q767, Q768	6Z-450 P.A. OUTPUT GATE.
Q769, Q770, Q771, Q772	6Z-450 P.A. OUTPUT GATE.
Q773, Q774, Q775, Q776	6Z-450 P.A. OUTPUT GATE.
Q777, Q778, Q779, Q780	6Z-450 P.A. OUTPUT GATE.
Q781, Q782, Q783, Q784	6Z-450 P.A. OUTPUT GATE.
Q785, Q786, Q787, Q788	6Z-450 P.A. OUTPUT GATE.
Q789, Q790, Q791, Q792	6Z-450 P.A. OUTPUT GATE.
Q793, Q794, Q795, Q796	6Z-450 P.A. OUTPUT GATE.
Q797, Q798, Q799, Q800	6Z-450 P.A. OUTPUT GATE.
Q801, Q802, Q803, Q804	6Z-450 P.A. OUTPUT GATE.
Q805, Q806, Q807, Q808	6Z-450 P.A. OUTPUT GATE.
Q809, Q810, Q811, Q812	6Z-450 P.A. OUTPUT GATE.
Q813, Q814, Q815, Q816	6Z-450 P.A. OUTPUT GATE.
Q817, Q818, Q819, Q820	6Z-450 P.A. OUTPUT GATE.
Q821, Q822, Q823, Q824	6Z-450 P.A. OUTPUT GATE.
Q825, Q826, Q827, Q828	6Z-450 P.A. OUTPUT GATE.
Q829, Q830, Q831, Q832	6Z-450 P.A. OUTPUT GATE.
Q833, Q834, Q835, Q836	6Z-450 P.A. OUTPUT GATE.
Q837, Q838, Q839, Q840	6Z-450 P.A. OUTPUT GATE.
Q841, Q842, Q843, Q844	6Z-450 P.A. OUTPUT GATE.
Q845, Q846, Q847, Q848	6Z-450 P.A. OUTPUT GATE.
Q849, Q850, Q851, Q852	6Z-450 P.A. OUTPUT GATE.
Q853, Q854, Q855, Q856	6Z-450 P.A. OUTPUT GATE.
Q857, Q858, Q859, Q860	6Z-450 P.A. OUTPUT GATE.
Q861, Q862, Q863, Q864	6Z-450 P.A. OUTPUT GATE.
Q865, Q866, Q867, Q868	6Z-450 P.A. OUTPUT GATE.
Q869, Q870, Q871, Q872	6Z-450 P.A. OUTPUT GATE.
Q873, Q874, Q875, Q876	6Z-450 P.A. OUTPUT GATE.
Q877, Q878, Q879, Q880	6Z-450 P.A. OUTPUT GATE.
Q881, Q882, Q883, Q884	6Z-450 P.A. OUTPUT GATE.
Q885, Q886, Q887, Q888	6Z-450 P.A. OUTPUT GATE.
Q889, Q890, Q891, Q892	6Z-450 P.A. OUTPUT GATE.
Q893, Q894, Q895, Q896	6Z-450 P.A. OUTPUT GATE.
Q897, Q898, Q899, Q900	6Z-450 P.A. OUTPUT GATE.
Q901, Q902, Q903, Q904	6Z-450 P.A. OUTPUT GATE.
Q905, Q906, Q907, Q908	6Z-450 P.A. OUTPUT GATE.
Q909, Q910, Q911, Q912	6Z-450 P.A. OUTPUT GATE.
Q913, Q914, Q915, Q916	6Z-450 P.A. OUTPUT GATE.
Q917, Q918, Q919, Q920	6Z-450 P.A. OUTPUT GATE.
Q921, Q922, Q923, Q924	6Z-450 P.A. OUTPUT GATE.
Q925, Q926, Q927, Q928	6Z-450 P.A. OUTPUT GATE.
Q929, Q930, Q931, Q932	6Z-450 P.A. OUTPUT GATE.
Q933, Q934, Q935, Q936	6Z-450 P.A. OUTPUT GATE.
Q937, Q938, Q939, Q940	6Z-450 P.A. OUTPUT GATE.
Q941, Q942, Q943, Q944	6Z-450 P.A. OUTPUT GATE.
Q945, Q946, Q947, Q948	6Z-450 P.A. OUTPUT GATE.
Q949, Q950, Q951, Q952	6Z-450 P.A. OUTPUT GATE.
Q953, Q954, Q955, Q956	6Z-450 P.A. OUTPUT GATE.
Q957, Q958, Q959, Q960	6Z-450 P.A. OUTPUT GATE.
Q961, Q962, Q963, Q964	6Z-450 P.A. OUTPUT GATE.
Q965, Q966, Q967, Q968	6Z-450 P.A. OUTPUT GATE.
Q969, Q970, Q971, Q972	6Z-450 P.A. OUTPUT GATE.
Q973, Q974, Q975, Q976	6Z-450 P.A. OUTPUT GATE.
Q977, Q978, Q979, Q980	6Z-450 P.A. OUTPUT GATE.
Q981, Q982, Q983, Q984	6Z-450 P.A. OUTPUT GATE.
Q985, Q986, Q987, Q988	6Z-450 P.A. OUTPUT GATE.
Q989, Q990, Q991, Q992	6Z-450 P.A. OUTPUT GATE.
Q993, Q994, Q995, Q996	6Z-450 P.A. OUTPUT GATE.
Q997, Q998, Q999, Q1000	6Z-450 P.A. OUTPUT GATE.

NOTES:

A. MATERIAL - ONE TWO EIGHT GLASS LAMINATE TYPE BA-10E  
COMPAR TUB, BOTH SIDES, TIME 70-042-000 PER MIL.-P.189A.  
SECTION AND INSIDE DOW PIPE SIZE, 1-1/2".  
SAMPLED FROM SPEC. S-162-P-3.  
UNUSABLE WHEN RECEIVED REQUIRED ON ALL HORIZONTALLY MOUNTED  
S&L MODULES TO BE INFILLED WITH AN G-LAMP FILM ON  
BOTTOM OF MODULE.

C.P. INDICATES REAR TIE RODS

TWOIL STRIPS -

A --- 082 DIA (70%)  
B --- 082 DIA (70%)  
C --- 082 DIA (70%)  
ALL OTHER OR DIA (70%)

B. ALL UNUSED MODULE LEADS TO EXTEND  
APPROX. 1' BEYOND BOARD AFTER  
MODULE INSTALLATION.



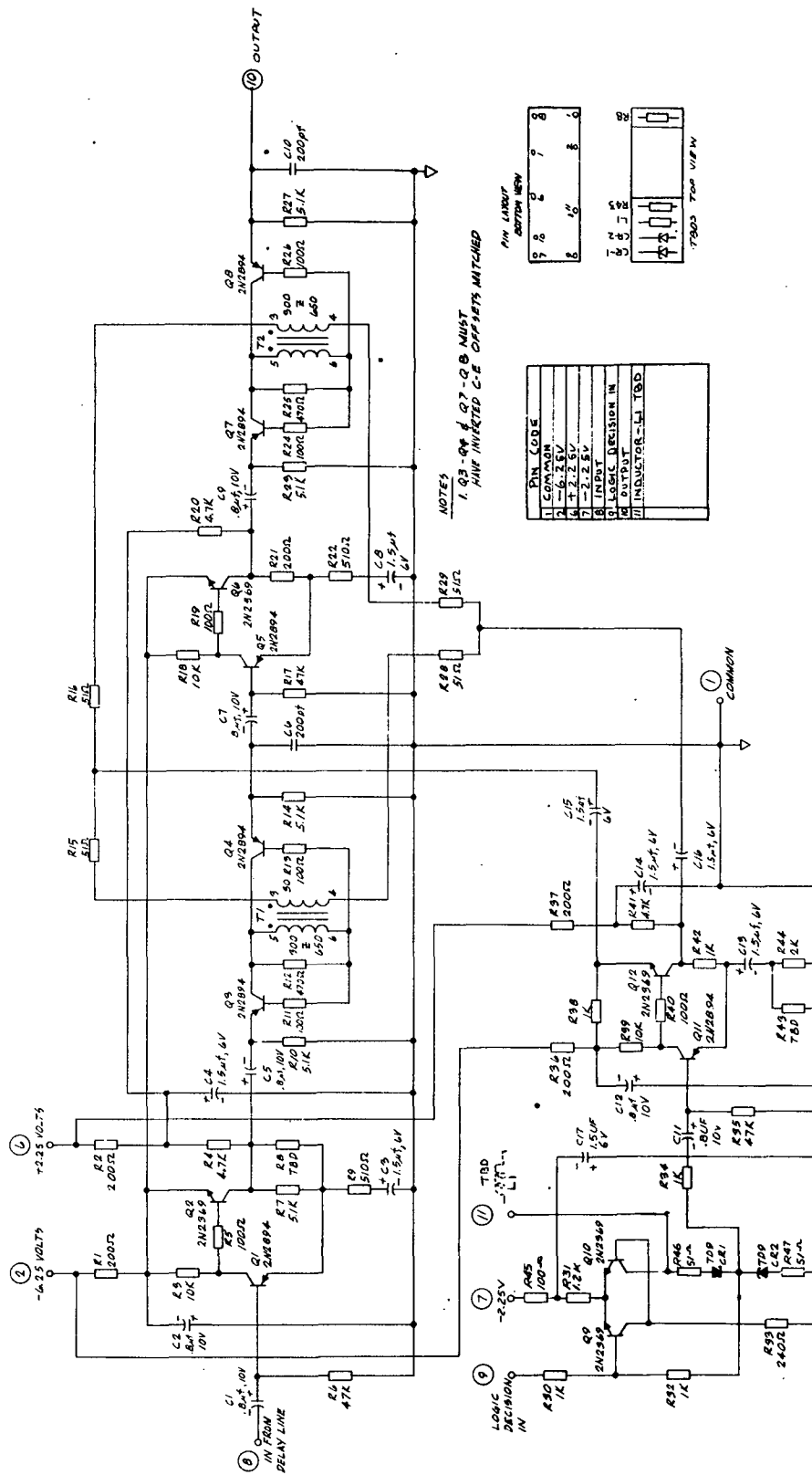


Figure 5. Linear Gate, Electrical Schematic Diagram

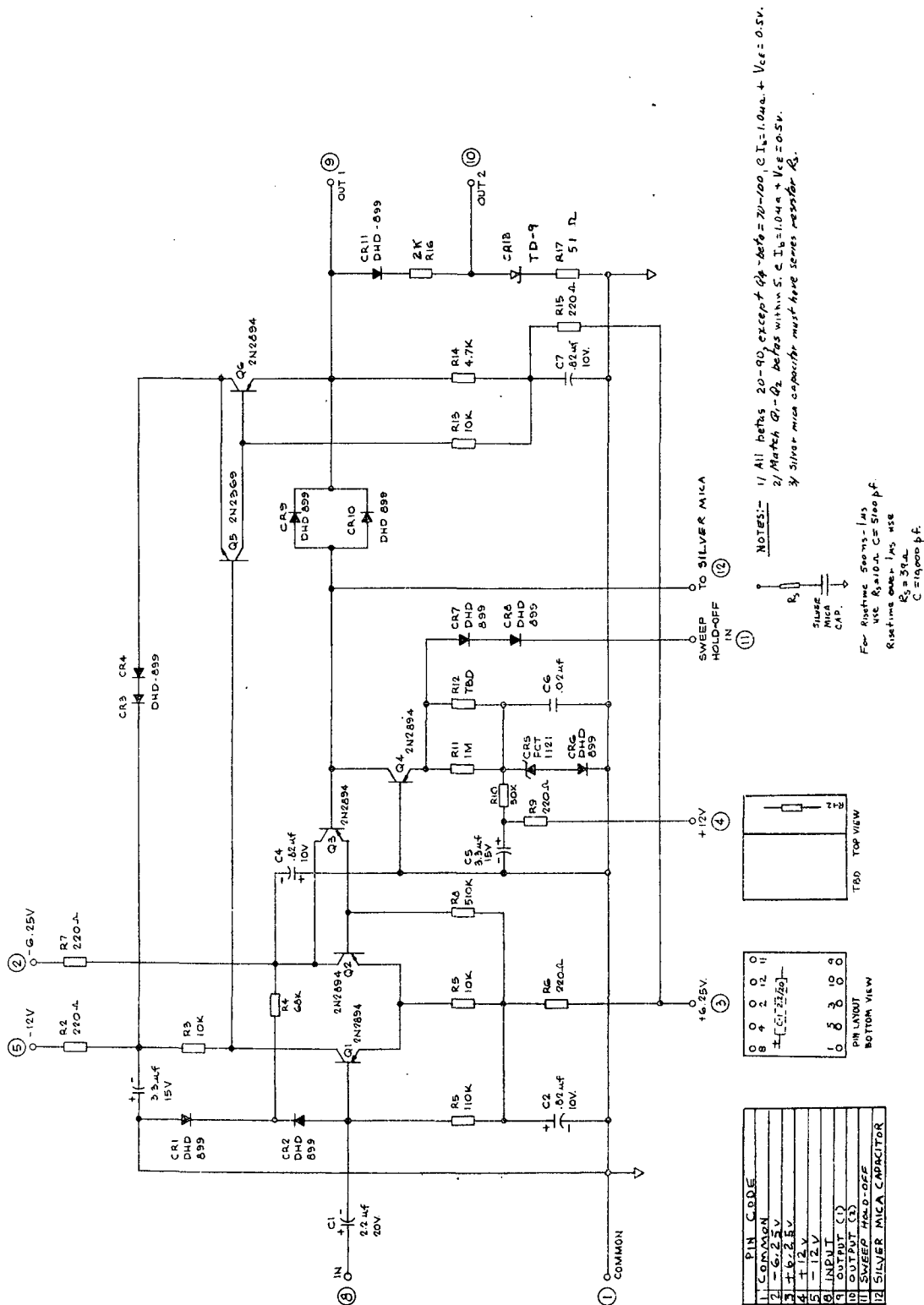
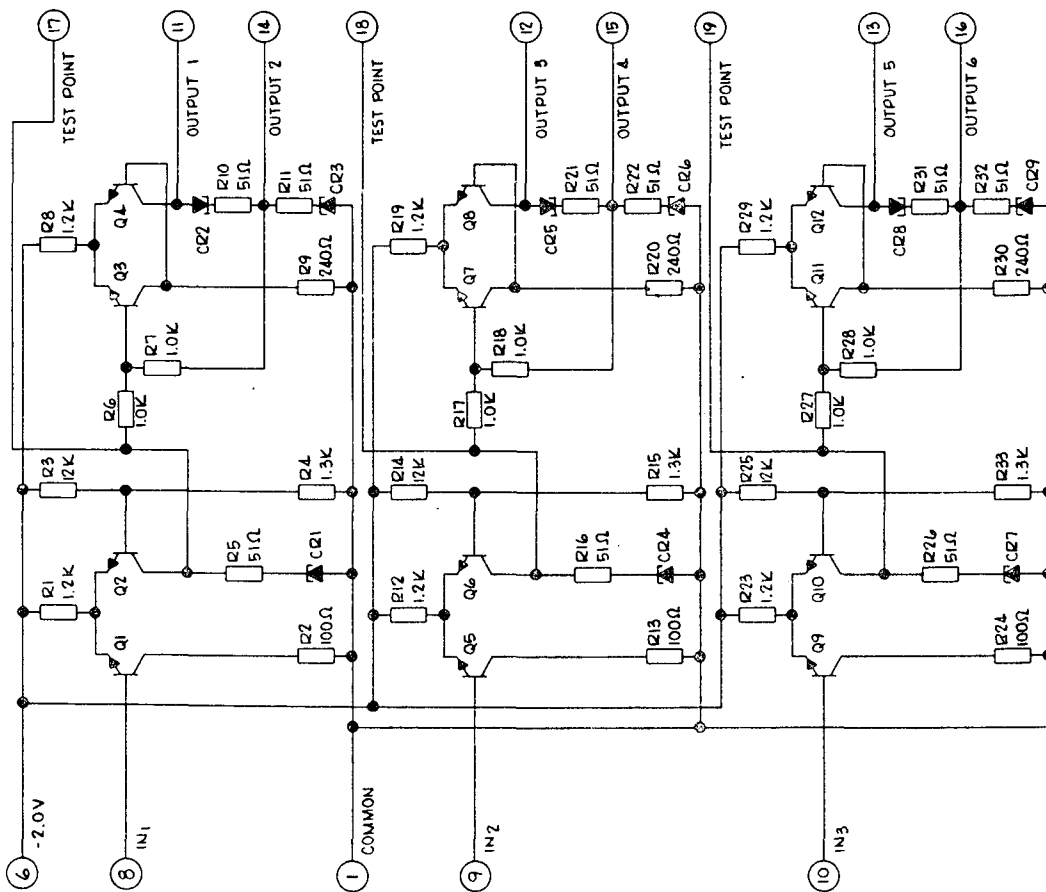


Figure 6. Sweep, Electrical Schematic Diagram





- NOTES:  
 UNLESS OTHERWISE NOTED  
 1. ALL RESISTORS ARE 1/4 W,  $\pm 5\%$  CARBON  
 2. ALL TRANSISTORS ARE 2N2369.  
 3. ALL DIODES ARE 1N60.

Figure 8. Threshold Detector and Pulser, Electrical Schematic Diagram

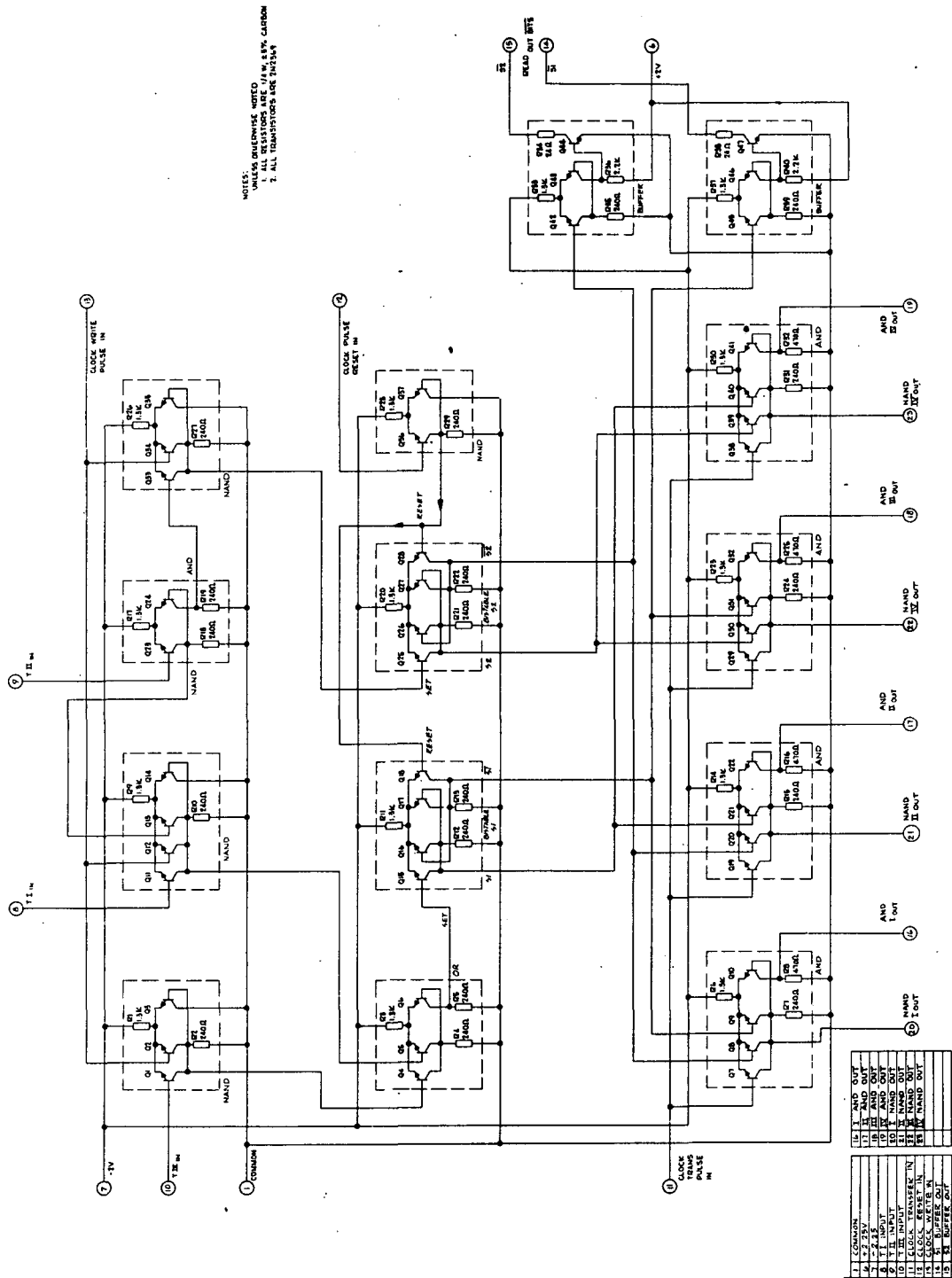


Figure 9. Four Range Decision Circuit, Electrical Schematic Diagram

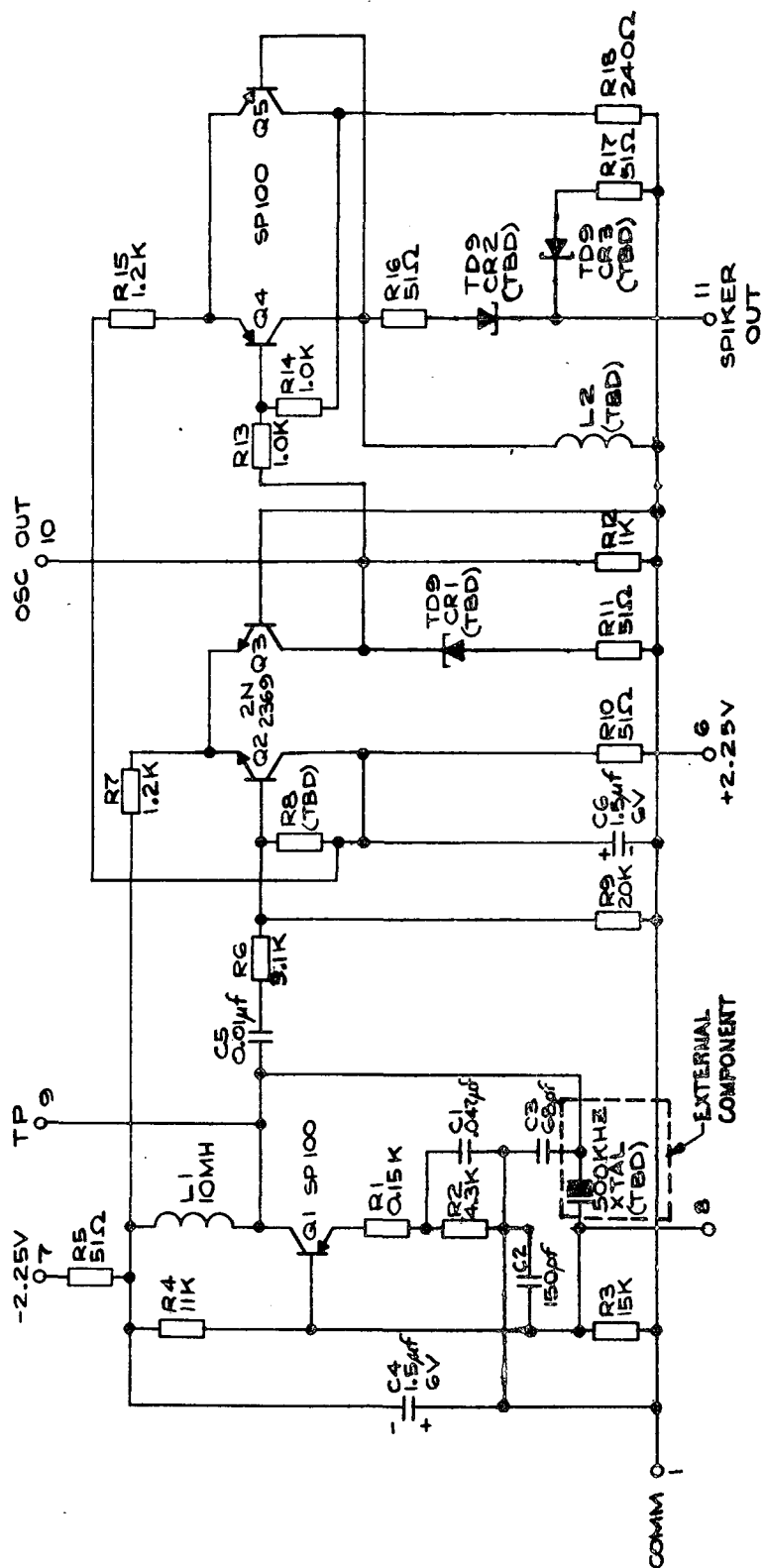


Figure 10. 500 kHz Square Wave Oscillator and Spiker, Electrical Schematic Diagram

**Figure 11. Clock and Buffer Circuits, Electrical Schematic Diagram**

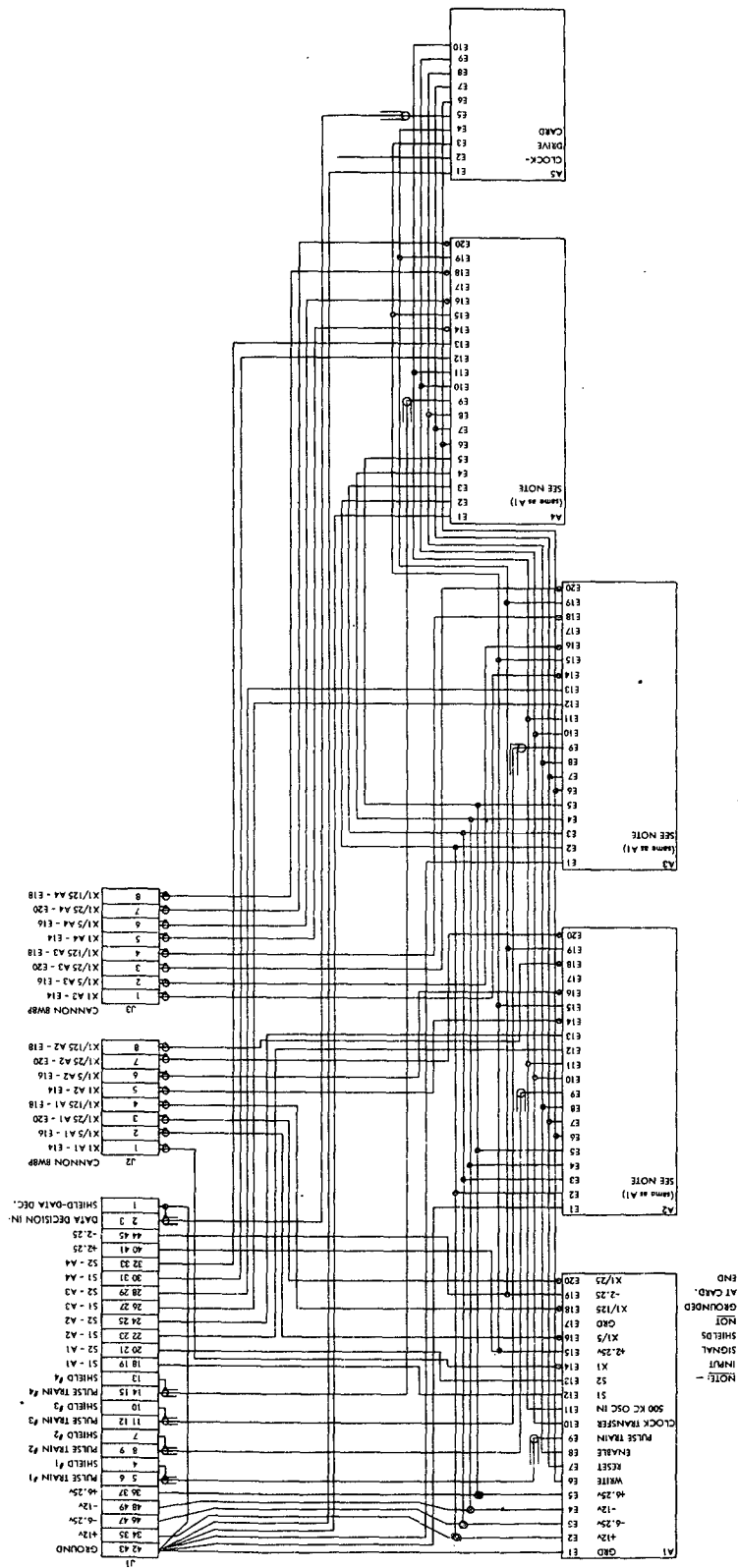


Figure 12. 10<sup>5</sup> Pulse Height Analyzer System Board Interconnections